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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/726,297	12/02/2003	Hong H. Chan	110350-133009	5246

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EXAMINER	
TON, MY TRANG	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 03/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/726,297	CHAN ET AL.	
	Examiner	Art Unit	
	My-Trang N. Ton	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-37 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) 22-27 is/are allowed.

6)☒ Claim(s) 1,2,6,11,14-16,19,28 and 33-37 is/are rejected.

7)☒ Claim(s) 3-5, 7-10,12,13,17,18,20,21 and 29-32 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 02 December 2003 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

MY-TRANG NU TON
PRIMARY EXAMINER

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 3/8/04.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

The disclosure is objected to because of the following informalities:

In page 5, line 22, before "strong", in order to avoid any confusion -- weak and – should be inserted.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

Claims 11, 19 and 34-37 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 11, the limitation "a first voltage control delay element responsive to an input signal to generate a signal to turn on the second stage and a second voltage control delay element responsive to the input signal and the control signal to generate a pulse signal to turn off the second stage" is misdescriptive of the present invention since such limitation is not seen as recited therein. In order to avoid any confusion, Applicant is required to particularly point out how these limitations read on the circuit arrangement of the drawings.

Claim 19 is similarly rejected as claim 11.

The method claim 34 is indefinite under 35 U.S.C. 112, second paragraph since it depends to the apparatus claim. In Ex parte Lyell, 17 USPQ2d 1548 (Bd. Pat. App. & Inter. 1990).

The method claims 35-37 are similarly rejected as claim 34.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-2, 14-16, 28 and 33 are rejected under 35 U.S.C. 102(b) as being anticipated by Ilkbahar et al (U.S Patent No. 5,898,321).

Ilkbahar et al disclose in Figs. 1-5 a slew rate control circuit including:

a driver (505) to drive an output signal (519) having a plurality of low-to-high and high-to-low signal transitions (LOW to HIGH and HIGH to LOW transitions), with each of the signal transitions having a clock-to-output delay;

a pre-driver (503) coupled to the driver (505), the pre-driver (503) having a first (531A – 531C, 547D-547F, 545D-545F) and a second stage (529A –529C, 545A-545C, 533A-533C, 547A-547C) to cooperatively generate a reshaped waveform to trigger the LH and HL signal transitions of the output signal (519), with the first stage (531A – 531C, 547D-547F, 545D-545F) generating an initial waveform and the second stage (529A –529C, 545A-545C, 533A-533C, 547A-547C) modifying the initial waveform to generate the reshaped waveform based at least in part on a difference in the clock-to-output delays of the LH and HL signal transitions as recited in claim 1.

Regarding claim 2: the first stage (531A – 531C, 547D-547F, 545D-545F) is capable of setting a slew rate for the driver and the second stage (529A –529C, 545A-

545C, 533A-533C, 547A-547C) is capable of changing the clock-to-output delay of one of the signal transitions of the output signal (519).

Regarding claim 14:

a driver (505) to generate an output signal (519) having a plurality of low-to-high and high-to-low signal transitions (L to H, H to L transitions);

a pre-driver (503) having a first (531A – 531C, 547D-547F, 545D-545F) and a second (529A –529C, 545A-545C, 533A-533C, 547A-547C) stage commonly coupled to the driver (505) and responsive to an input signal (117) to generate a pre-driver waveform to trigger the LH signal transitions after a LH switching delay period and to trigger the HL signal transitions after a HL switching delay period;

a compensator circuit (115) coupled to the driver (505) to measure a quantity reflective of a difference between the LH and HL switching delay periods; and

the second stage in communications with the compensator circuit to modify the pre-driver waveform during an adjustment period based upon the measured quantity, the adjustment period occurring during at least a portion of one of the switching delay periods (the second stage 529A –529C, 545A-545C, 533A-533C, 547A-547C in communications with the compensator circuit 115 is capable of performing the function as recited therein).

Regarding the limitation recited in claim 15: the second state (529A –529C, 545A-545C, 533A-533C, 547A-547C) is capable of adjusting the rate of voltage change of the pre-driver waveform during the adjustment period.

Regarding claim 16: the compensator circuit (115) is capable of performing the function as recited therein.

Claim 28 is similarly rejected as claim 1. Moreover, the limitations "a selected one of a graphics and a video controller; a bus coupled to the selected one of the graphic and video controller" are seen to define intended use. The circuit of Ilkbahar et al is capable of using in the system including a graphics, a video controller and a bus as recited. **In re Tuominen, 213 USPQ 89 (CCPA 1982) & In re Pearson, 494 F.2d 1399, 181 USPQ 641 (CCPA 1974).**

The limitation recited in claim 33 is similarly rejected as claim 14.

Claims 1-2, 6, 14-16, 28 and 33 are similarly rejected under 35 U.S.C. 102(b) as being anticipated by Muljono et al (U.S Patent No. 6,538,464).

Muljono et al disclose in Figs. 1-5 a slew rate control circuit including:

a driver (505) to drive an output signal (519) having a plurality of low-to-high and high-to-low signal transitions (LOW to HIGH and HIGH to LOW transitions), with each of the signal transitions having a clock-to-output delay;

a pre-driver (503) coupled to the driver (505), the pre-driver (503) having a first (531A – 531C, 547D-547F, 545D-545F) and a second stage (529A –529C, 545A-545C, 533A-533C, 547A-547C) to cooperatively generate a reshaped waveform to trigger the LH and HL signal transitions of the output signal (519), with the first stage (531A – 531C, 547D-547F, 545D-545F) generating an initial waveform and the second stage (529A –529C, 545A-545C, 533A-533C, 547A-547C) modifying the initial waveform to

generate the reshaped waveform based at least in part on a difference in the clock-to-output delays of the LH and HL signal transitions as recited in claim 1.

Regarding claim 2: the first stage (531A – 531C, 547D-547F, 545D-545F) is capable of setting a slew rate for the driver and the second stage (529A –529C, 545A-545C, 533A-533C, 547A-547C) is capable of changing the clock-to-output delay of one of the signal transitions of the output signal (519).

Regarding claim 6: element 119 reads on a voltage supply.

Regarding claim 14:

a driver (505) to generate an output signal (519) having a plurality of low-to-high and high-to-low signal transitions (L to H, H to L transitions);

a pre-driver (503) having a first (531A – 531C, 547D-547F, 545D-545F) and a second (529A –529C, 545A-545C, 533A-533C, 547A-547C) stage commonly coupled to the driver (505) and responsive to an input signal (117) to generate a pre-driver waveform to trigger the LH signal transitions after a LH switching delay period and to trigger the HL signal transitions after a HL switching delay period;

a compensator circuit (115) coupled to the driver (505) to measure a quantity reflective of a difference between the LH and HL switching delay periods; and

the second stage in communications with the compensator circuit to modify the pre-driver waveform during an adjustment period based upon the measured quantity, the adjustment period occurring during at least a portion of one of the switching delay periods (the second stage 529A –529C, 545A-545C, 533A-533C, 547A-547C in

communications with the compensator circuit 115 is capable of performing the function as recited therein).

Regarding the limitation recited in claim 15: the second state (529A –529C, 545A-545C, 533A-533C, 547A-547C) is capable of adjusting the rate of voltage change of the pre-driver waveform during the adjustment period.

Regarding claim 16: the compensator circuit (115) is capable of performing the function as recited therein.

Claim 28 is similarly rejected as claim 1. Moreover, the limitations "a selected one of a graphics and a video controller; a bus coupled to the selected one of the graphic and video controller" are inherent seen in Figs. 9-10 of Muljono et al.

The limitation recited in claim 33 is similarly rejected as claim 14.

Allowable Subject Matter

Claims 3-5, 7-10, 12-13, 17-18, 20-21, 29-32 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art disclosed or suggested to show the particular structure and/or the particular operation recited in these claims namely: "a compensator circuit ... to provision of a feedback in a form of a control signal ..." as recited in claim 3; "a compensator circuit to generate a control signal having a feedback ..." as recited in claim 7; "a pattern generator ... between the first and second test output signals to generate the control signal" as recited in claim 9; "a pre-driver control circuit ... in response to the measured quantity" as recited in claim 17; "a pattern generator ... to generate the measured

quantity" as recited in claim 20; "a compensator circuit" in combination with "a control circuit" as recited in claim 29.

Claims 22-27 are allowable over the prior art of record. None of the prior art disclosed or suggested to show the particular structure and/or the particular operation recited in these claims namely: the combination of "a pattern generator", "a first and second weak pre-driver stage", "a first and a second driver", "a compensator circuit" and "a first and a second strong pre-driver stage" as recited in claim 22.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to My-Trang N. Ton whose telephone number is 571-272-1754. The examiner can normally be reached on 7:00 a.m - 5:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

My-Trang N. Ton
Primary Examiner
Art Unit 2816
3/21/05